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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,781	04/09/2004	Shunpei Yamazaki	0756-7289	8829

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,781	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-42 and 45-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-42 and 45-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed on 1/12/06. Currently, claims 33-42 and 45-63 are pending.

Election/Restrictions

Applicant's election without traverse of claims 33-36, 41, 42 and 45-63 in the reply filed on 1/12/06 is acknowledged. Applicant has cancelled non-elected claims.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 4/09/04, 9/27/04, and 8/31/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 33-42, 45-63 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka US Patent 5,893,990.

Tanaka discloses the semiconductor method as claimed. See figures 1-13 and corresponding text, where Tanaka teaches, pertaining to claim 33, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **76** by irradiating an energy beam output continuously while scanning the energy beam to a semiconductor film (figure 7C; col. 9, lines 55-59); forming a gate electrode **106** over the crystalline semiconductor film (figure 10B; col. 11, lines 10-15 and 39-56); and forming an impurity region **111/113/114/112** in the crystalline semiconductor film using the gate electrode as a mask (figure 11B; col. 12, lines 15-24), wherein a scanning direction of the beam changes outside an element-forming region formed with the crystalline semiconductor film (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claim 34, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **76** by irradiating an energy beam output continuously while scanning the energy beam to a semiconductor film (figure 7C; col. 9, lines 55-59); forming a gate electrode **106** over the crystalline semiconductor film (figure 10B; col. 11, lines 10-15 and 39-56); and forming an impurity region **111/113/114/112** in the crystalline semiconductor film using the gate electrode as a mask (figure 11B; col. 12, lines 15-24), wherein the beam is irradiated to an outside of the element-forming region formed with the crystalline semiconductor film when the beam starts to be irradiated or the beam ends to be irradiated (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claims 35 and 36, wherein scanning the energy beam is performed by using a galvanometer mirror or a polygon mirror (figures 2 and 4; col. 6, lines 62-67; col. 7, lines 5-12).

Tanaka teaches, pertaining to claims 37 and 38, wherein the energy beam output continuously is a beam emitted from a laser selected from the group consisting of a YVO_4 laser, a YAG laser, a YLF laser, a $YALO_3$ laser, and an Ar laser (col. 2, lines 1-5).

Tanaka teaches, pertaining to claims 39 and 40, wherein the element-forming region is a region where a display device or an integrated circuit is formed (col. 11, lines 10-15).

Tanaka teaches, pertaining to claim 41, a method for manufacturing a semiconductor device comprising the steps of: forming a semiconductor film **73** over a substrate **71** (figure 7A; col. 9, lines 22-26); crystallizing the semiconductor film **76** by irradiating an energy beam output continuously while scanning the energy beam to the semiconductor film (figure 7C; col. 9, lines 55-59); forming a plurality of semiconductor islands by patterning the crystallized semiconductor film (figures 8A-8D; col. 10, lines 23-32); forming a first circuit **100** using one of the plurality of semiconductor islands over the substrate (figures 11A-C ; col. 13, lines 19-29); and forming a second circuit **100** using another one of the plurality of semiconductor islands over the substrate ((figures 11A-C ; col. 13, lines 19-29), wherein the energy beam is not irradiated to the first circuit and the second circuit whiling changing a scanning direction of the energy beam (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claim 42, wherein the energy beam is irradiated to a region between the first circuit and the second circuit while changing the scanning direction of the energy beam (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claims 45-47, wherein the semiconductor device is incorporated into at least one selected from the group consisting of a display, a mobile computer, a game machine, and an electronic book reader (col. 11, lines 10-15).

Tanaka teaches, pertaining to claim 48, wherein scanning the energy beam is performed by using a galvanometer mirror or a polygon mirror (figures 2 and 4; col. 6, lines 62-67; col. 7, lines 5-12).

Tanaka teaches, pertaining to claim 49, wherein the energy beam output continuously is a beam emitted from a laser selected from the group consisting of a YVO_4 laser, a YAG laser, a YLF laser, a $YALO_3$ laser, and an Ar laser (col. 2, lines 1-5).

Tanaka teaches, pertaining to claim 50, a method for manufacturing a semiconductor device comprising the steps of: forming a semiconductor film **73** over a substrate **71** (figure 7A; col. 9, lines 22-26); crystallizing the semiconductor film **76** by irradiating an energy beam output continuously while scanning the energy beam to the semiconductor film (figure 7C; col. 9, lines 55-59); forming a plurality of semiconductor islands by patterning the crystallized semiconductor film (figures 8A-8D; col. 10, lines 23-32); forming a first circuit **100** using one of the plurality of semiconductor islands over the substrate (figures 11A-C ; col. 13, lines 19-29); and forming a second circuit **100** using another one of the plurality of semiconductor islands over the substrate ((figures 11A-C ; col. 13, lines 19-29), wherein the energy beam is not irradiated to the first circuit and the second circuit when the beam starts to be irradiated or the beam ends to be irradiated (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claim 51, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **76** by irradiating an energy

beam output continuously while scanning the energy beam to a semiconductor film by moving the semiconductor film and the energy beam relatively (figure 7C; col. 9, lines 55-59); forming a gate electrode **106** over the crystalline semiconductor film (figure 10B; col. 11, lines 10-15 and 39-56); and forming an impurity region **111/113/114/112** in the crystalline semiconductor film using the gate electrode as a mask (figure 11B; col. 12, lines 15-24), wherein a scanning direction of the beam changes outside an element-forming region formed with the crystalline semiconductor film (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claim 52, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **76** by irradiating an energy beam output continuously while scanning the energy beam to a semiconductor film by moving the semiconductor film and the energy beam relatively (figure 7C; col. 9, lines 55-59); forming a gate electrode **106** over the crystalline semiconductor film (figure 10B; col. 11, lines 10-15 and 39-56); and forming an impurity region **111/113/114/112** in the crystalline semiconductor film by using the gate electrode as a mask(figure 11B; col. 12, lines 15-24), wherein the bema is irradiated to an outside of the element-forming region formed with the crystalline semiconductor film when the beam starts to be irradiated (figures 8A-9; col. 10, lines 36-42 and 52-62).

Tanaka teaches, pertaining to claims 53, 56 and 60, wherein scanning the energy beam is performed by using a galvanometer mirror or a polygon mirror (figures 2 and 4; col. 6, lines 62-67; col. 7, lines 5-12).

Tanaka teaches, pertaining to claims 54, 57 and 61, wherein the energy beam output continuously is a beam emitted from a laser selected from the group consisting of a YVO_4 laser, a YAG laser, a YLF laser, a $YALO_3$ laser, and an Ar laser (col. 2, lines 1-5).

Tanaka teaches, pertaining to claims 58 and 62, wherein the element-forming region is a region where a display device or an integrated circuit is formed (col. 11, lines 10-15).

Tanaka teaches, pertaining to claims 55, 59 and 63, wherein the semiconductor device is incorporated into at least one selected from the group consisting of a display, a mobile computer, a game machine, and an electronic book reader (col. 11, lines 10-15).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent examiner
March 5, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER